REMARKS

Claims 1-11 were examined and reported in the Office Action. Claims 1, 2, 4, 5, 10 and 11 are rejected. Claims 1, 3, 4, 6 and 8 are amended. Claims 1-11 remain. It is asserted in the Office Action that Applicant has yet to file a certified copy of the Republic of Korea 2003-86257 application. Applicant has filed the certified copy as mailed on July 2, 2004, with return postcard dated July 7, 2004 by the U.S.P.T.O. If necessary, Applicant will submit the filed documents and copy of the returned post card.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 103(a)

A. It is asserted in the Office Action that claims 1, 2, 4, 5 and 10 - 11 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent 6,636,443 issued to Kang ("Kang") in view of U. S. Patent 6,192,429 issued to Jeong et al. ("Jeong"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Applicant's amended claim 1 contains the limitations of

> [a]n address input buffer in a semiconductor memory device, comprising: a differential amplifying means for differentially amplifying a reference voltage and an external address signal; and a controlling means for generating a bias

> control signal by receiving a refresh signal and a bank active signal to control the differential amplifying means, wherein activation of the bias control signal depends on the bank active signal when the refresh signal is abnormally activated in an initialization process.

Applicant's amended claim 4 contains the limitations of

> [a]n address buffer in a semiconductor memory device, comprising: a differential input unit receiving a reference voltage and an address signal; a current mirroring unit connected between the differential input unit and a first voltage; a biasing unit, which is connected between the differential input unit and a second voltage, for supplying bias current to the differential input unit and the current mirroring unit; and a controlling unit for generating a bias control signal by receiving a refresh signal and a bank active signal to enable/disable the biasing unit, wherein the bias control signal is activated if the refresh signal is abnormally activated in an initialization process.

In other words, Applicant's claimed invention prevents erroneous operation in an initialization process and minimizes current consumption. When a refresh signal is abnormally activated in the initialization process, an activation of a bias control signal depends on a bank active signal (see paragraph [0039] of Applicant's specification, 'D' case in Table 1). Therefore, in Applicant's claimed invention the erroneous operation of the initialization process can be prevented.

Kang discloses a semiconductor memory device having row buffers capable of transmitting cell array data from DRAM including the row buffer to the external by one command. Kang, however, does not teach, disclose or suggest the limitations of claim 1 of

a controlling means for generating a bias control signal by receiving a refresh signal and a bank active signal to control the differential amplifying means, wherein activation of the bias control signal depends on the bank active signal when the refresh signal is abnormally activated in an initialization process.

or the limitations of claim 4 of

a controlling unit for generating a bias control signal by receiving a refresh signal and a bank active signal to enable/disable the biasing unit, wherein the bias control signal is

activated if the refresh signal is abnormally activated in an initialization process.

Jeong discloses integrated circuit memory devices that include a data input/output mask input buffer. Jeong, however, does not teach, disclose or suggest the limitations of claim 1 of

a controlling means for generating a bias control signal by receiving a refresh signal and a bank active signal to control the differential amplifying means, wherein activation of the bias control signal depends on the bank active signal when the refresh signal is abnormally activated in an initialization process.

or the limitations of claim 4 of

a controlling unit for generating a bias control signal by receiving a refresh signal and a bank active signal to enable/disable the biasing unit, wherein the bias control signal is activated if the refresh signal is abnormally activated in an initialization process.

Further, if one were to combine the teachings of Kang and Jeong, the result would include a refresh signal and a power down signal that are connected with a logic gate NOR. Then an output of the logic gate NOR and other signals are connected with a logic gate AND. The logic gate AND would then output a bias enable signal, which corresponds to the bias control signal of Applicant's claimed invention (see Applicant's specification, column 4, lines 58-66). Therefore, if the refresh signal is in a logic level high, the output of the logic gate NOR is always in a logic level low. Accordingly, an output of the logic gate AND, i.e., the bias control signal, is always in a logic level low. Therefore, even if the refresh signal is abnormally activated in the initialization process, the bias enable signal is inactivated. Thus, the erroneous operation of the initialization process cannot be prevented in such a combination.

Since neither Kang, Jeong, and therefore, nor the combination of the two teach, disclose or suggest all the limitations of Applicant's amended claims 1 and 4, as listed above, Applicant's amended claims 1 and 4 are not obvious over Kang in view of Jeong since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1 and 4, namely claims 2, and

5 and 11-11, respectively, would also not be obvious over Kang in view of Jeong for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 1-2, 4-5 and 10-11 are respectfully requested.

II. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 3 and 6-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-11, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-23 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: October 31, 2005

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on October 31, 2005.

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Jean Svoboda